The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANKLIN M. BAEZ

Appeal 2007-2016
Application 09/148,392
Technology Center 2100

Decided: September 10, 2007

Before KENNETH W. HAIRSTON, MAHSHID D. SAADAT, and SCOTT R. BOALICK, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a Final Rejection of claims 1-20 and 22-29, which are all of the claims pending in this application, as claim 21 has been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

Appellant has invented a method and a computer product for determining optimal values of design parameters of a subsystem to meet design constraints (Specification 3). The design parameters are optimized based on the parameter functions to satisfy the design constraints (*id.*).

Claim 1, which is representative of the claims on appeal, reads as follows:

1. A method comprising:

(a) creating parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, the parameter functions representing a relationship among design parameters of the subsystem, the design parameters including constraint and optimizing sets;

(b) selecting initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and

(c) selecting new design points on the parameter functions such that the second sum is improved with the design constraints.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Jyu	US 5,880,967	Mar. 9, 1999

The Examiner rejected claims 1-20 and 22-29 under 35 U.S.C. § 102(e) as anticipated by Jyu.[1]

We reverse.

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[1] The rejection over Jyu is the only rejection remaining before this panel as the Examiner has withdrawn the other rejections indicated in the Final Rejection in a Supplemental Answer, filed March 17, 2006 (Suppl. Answer 4).

ISSUE

Appellant contends that Jyu's transistor autosizing requires selecting an entire circuit and does not disclose 1) design points on a parameter function; 2) a parameter function having a first sum of a constraint set and a second sum of an optimizing set; 3) selecting the initial design points; and 4) selecting the new design points, as recited in the claims (Reply Br. 9-10). The Examiner asserts that the portions of Jyu relied on in the rejection "are all directed to analysis and improving the design using power and delay as the constraining factors with scaling up and down based on costing function responsive to changes in delay and/or power to yield an improved circuit" (Suppl. Answer 17). The Examiner further argues that Appellant is using well known technologies and methodologies to affect designs within a circuit framework (*id.*).

The issue, therefore, is whether the Examiner erred in rejecting the claims under 35 U.S.C. § 102(e). The issue specifically turns on whether Jyu anticipates Appellant's claimed invention by disclosing "selecting initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints," as recited in claim 1.

FINDINGS OF FACT

The following findings of fact (FF) are relevant to the issue involved in the appeal and are believed to be supported by a preponderance of the evidence.

1. Jyu relates to a method for minimizing signal delay and power consumption through combined power simulation and delay analysis resulting in iterative transistor resizing (Abstract). The method includes sizing up a first transistor when its time delay normalized to the time delay of greatest value exceeds a predetermined threshold value, and sizing down the transistor when the normalized time delay is less than the predetermined threshold value (col. 3, ll. 50-62).

2. Jyu provides for "Design goals" commands that facilitate three execution modes of the transistor autosizing engine 320: requirement mode, cost-function mode and slack-driven mode (default is cost-function mode). In requirement mode, delay and power form the two requirement parameters. If the delay requirement is specified (delay requirement mode), engine 320 will first satisfy the specified delay and then minimize the power. Conversely, if the power requirement is specified (power requirement mode), engine 320 will first satisfy the specified power and then minimize the delay. If both delay and power requirements are specified, the latter will overwrite the former. In other words, the last requirement command in the procedure will be executed and all previous requirement commands will be ignored (col. 10. ll. 52-66).

3. As depicted in Figure 6 of Jyu, an initial circuit must be selected in block 630 and controlled by the "design goals" commands, which provide for three execution modes: requirement mode, cost-function mode and slack-driven mode. In general, the circuit associated with the "best" size for the controlling execution mode is chosen as the initial circuit and

forwarded to second run-core block 316 (FIG. 3) in block 632 (FIG. 6) (col. 15, ll. 25-34).

4. Jyu further discloses that transistor autosizing engine 320 can characterize the delay and power performance of all the cells given a conventional, predefined cell library in which there are different sized cells for the same functionality. Based on this characterization and an evaluation of the values, engine 320 can select the appropriate cell(s) to reduce the delay and power, subject to the requirements of the user (col. 27, ll. 59-65).

PRINCIPLES OF LAW

1. Anticipation

A rejection for anticipation requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. *See Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

2. Burdens of Proof and Production

The examiner bears the burden of presenting at least a prima facie case of anticipation. *In re King*, 801 F.2d 1324, 1327, 231 USPQ 136, 138-39 (Fed. Cir. 1986); *In re Wilder*, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). Only if that burden is met, does the burden of going forward shift to the applicant. *In re King*, 801 F.2d at 1327, 231 USPQ at 138-39; *In re Wilder*, 429 F.2d at 450, 166 USPQ at 548.

Once a prima facie case is established and rebuttal evidence is submitted, the ultimate question becomes whether, based on the totality of the record, the examiner carried his burden of proof by a preponderance. *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

ANALYSIS

As described above, the portions of Jyu relied on by the Examiner, actually require selecting an initial circuit to start with, which is different from the claimed selecting initial design points on the parameter functions. As argued by Appellant (Reply Br. 9), Jyu selects the entire circuit instead of selecting design points on a parameter function (FF 3-4). We also disagree with the Examiner that because Jyu relates to analyzing and improving the design using power and delay as the constraining factors for the transistor size (Suppl. Answer 17), the claimed subject matter is met. What is missing from the Examiner's analysis is a discussion of how these elements are used in the design and how the constraint and optimization in Jyu is used in the same way as in the claims.

Additionally, absent proper evidence to support the Examiner's position (Answer 17), we remain unconvinced that the technologies and methodologies employed by Appellant are well known. Satisfying the initial burden of presenting a prima facie case of anticipation requires more than making conclusory statements that one of ordinary skill in the art would have always designed the constraints and used a first sum of the constraint

set and a second sum of the optimization set. While the Examiner's extensive explanation of the knowledge of one of ordinary skill in the art in the Supplemental Answer is noted, the Examiner's Answer is not prior art. The prior art is Jyu, and it does not indicate that such analysis and design improvement in the manner recited in the claims is well known in the art, nor does it suggest the inherency of such features. *See In re Yates*, 663 F.2d 1054, 211 USPQ 1149, 1151 (CCPA 1981) (when the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference).

The Examiner refers to the use of constraints and optimization in Jyu and finds their use in designing a transistor size based on computing power to be the same as the claimed first sum and the second sum (Suppl. Answer 18). While the transistor in Jyu is sized to satisfy both delay and power, we agree with Appellant (Reply Br. 11) that it is not "inherent" or "well known" to do so based on selecting initial design points on the parameter functions having a first sum of the constraints set and a second sum of the optimizing set. Nor has the Examiner identified in Jyu the ways to satisfy the design constraints by a first sum of the constraint set, explicitly or implicitly. Therefore, as the initial burden is not met by the Examiner, the burden of going forward in rebuttal does not shift to Appellant. We also note Appellant's effort to address the Examiner's position to the extent that such position can be understood.

Under the facts we have here and the arguments presented by the Examiner and Appellant, as described above, we have concluded that a prima facie case has not been established.

CONCLUSION

On the record before us, we find that the Examiner fails to make a prima facie case that Jyu anticipates claim 1 or the other independent claims 11, 22, and 28, which include similar limitations. Therefore, in view of our analysis above, the 35 U.S.C. § 102 rejection of claims 1-20 and 22-29 as anticipated by Jyu cannot be sustained.

DECISION

The decision of the Examiner rejecting claims 1-20 and 22-29 under 35 U.S.C. § 102 is reversed.

REVERSED

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